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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/424,670 | 05/11/2000 | Yoichi Hijikata | 104824 | 7939 |

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| EXAMINER | |
|---|---|
| WILSON, YOLANDA L | |
| ART UNIT | PAPER NUMBER |
| 2113 | |

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/424,670 | HIJIKATA, YOICHI | |
| | Examiner | Art Unit | |
| | Yolanda Wilson | 2113 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## FINAL DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Swoboda (USPN 5828824A). As appears in claim 1, Swoboda discloses a central processing unit formed to be switchable between said user mode and said debugging mode, for executing instructions in each of said user mode and said debugging mode in column 9, lines 8-23.

Swoboda discloses a switch that switches said central processing unit from said user mode to said debugging mode when a forced break is input through a terminal that is not used in said user mode in column 4, lines 66-67 – column 5, lines 1-2.

3. As per claim 2, Swoboda discloses said microcomputer has an on-chip debugging function and comprises a debugging terminal connected to a communications line for transferring debugging information that is used for on-chip debugging to and from an external debugging tool; and a forced break is input through said debugging terminal in column 9, lines 8-40 and column 4, lines 66-67 – column 5, lines 1-2.

4. As per claim 3, Swoboda discloses said microcomputer comprises a first monitor means that transfers data to and from a second monitor means determining a primitive command to be executed according to said data received from said second monitor means and executing the determined primitive command said second monitor being provided outside said microcomputer for converting a debugging command into at least one primitive command; a single communications line for transferring said data in a half-duplex bi-directional manner is connected to said debugging terminal; said central processing unit executes a user program when in said user mode and executes said primitive command when in said debugging mode in column 8, 51-67 – column 9, line 1; column 9, lines 8-40.

Swoboda discloses said switch switches said central processing unit from said user mode to said debugging mode when a forced break is input through said debugging terminal in column 4, lines 66-67 – column 5, lines 1-2.

5. As per claim 4, Swoboda discloses a holder that holds a terminal for the input of a forced break at a first level which is either one of high and (should be or) low during a state in which no external debugging tool is connected in column 7, lines 5-14. Swoboda discloses wherein said central processing unit starts execution in said user mode when said terminal for inputting said forced break is at a time of reset or starts execution in said debugging mode when said terminal for inputting said forced break is not at said first level at a time of reset in column 20, lines 49-52.

6. As per claim 5, Swoboda discloses a holder that holds a terminal for the input of a forced break at a first level which is either one of high and (should be or) low during a state in which no external debugging tool is connected, wherein said central processing unit starts execution in said user mode when said terminal for inputting said forced break is at a time of reset or starts execution in said debugging mode when said terminal for inputting said forced break is not at said first level at a time of reset in column 20, lines 49-52.

7. As per claim 6, Swoboda discloses a holder that holds a terminal for the input of a forced break at a first level which is either one of high and (should be or) low during a state in which no external debugging tool is connected, wherein said central processing unit starts execution in said user mode when said terminal for inputting said forced break is at a time of reset or starts execution in said debugging mode when said terminal for inputting said forced break is not at said first level at a time of reset in column 20, lines 49-52.

8. As per claim 7, Swoboda discloses the microcomputer of claim 1; an input source of data that is to be a processing object of said microcomputer; and an output device for outputting data that has been processing by said microcomputer column 9, lines 8-23; column 4, lines 66-67 – column 5, lines 1-2.

9. As per claim 8, Swoboda discloses the microcomputer of claim 2; an input source of data that is to be a processing object of said microcomputer; and an output device for outputting data that has been processing by said microcomputer in column 9, lines 8-40 and column 4, lines 66-67 – column 5, lines 1-2.

10. As per claim 9, Swoboda discloses the microcomputer of claim 3; an input source of data that is to be a processing object of said microcomputer; and an output device for outputting data that has been processing by said microcomputer in column 8, 51-67 – column 9, line 1; column 9, lines 8-40; column 4, lines 66-67 – column 5, lines 1-2.

11. As per claim 10, Swoboda discloses the microcomputer of claim 4; an input source of data that is to be a processing object of said microcomputer; and an output device for outputting data that has been processing by said microcomputer in column 20, lines 49-52.

12. As per claim 11, Swoboda discloses the microcomputer of claim 5; an input source of data that is to be a processing object of said microcomputer; and an output device for outputting data that has been processing by said microcomputer in column 20, lines 49-52.

13. As per claim 12, Swoboda discloses the microcomputer of claim 6; an input source of data that is to be a processing object of said microcomputer; and an output device for outputting data that has been processing by said microcomputer in column 20, lines 49-52.

14. As per claim 13, a second monitor that performs processing for converting a debugging command developed by a host system into at least one primitive command; a first monitor that transfers data to and from said second monitor determining a primitive command to be executed according to said data received from said second monitor and executing the determined primitive command; a debugging terminal not used in said user mode and provided on a chip including

said central processing unit and connected to a single communications line for transferring said data in a half-duplex bi-directional manner in said debugging mode in column 8, 51-67 – column 9, line 1; column 9, lines 8-40.

Swoboda discloses a switch that switches said central processing unit from said user mode to said debugging mode when a forced break is input through said debugging terminal in column 4, lines 66-67 – column 5, lines 1-2.

***Response to Arguments***

15. Applicant's arguments filed June 10, 2004 have been fully considered but they are not persuasive. The arguments presented by Applicant include 'Applicant asserts that Swoboda does not disclose or suggest a microcomputer, including at least a switch that switches a central processing unit from a user mode to a debugging mode when a forced bread is input through a terminal that is not used in the user mode, as recited in independent claim 1 and similarly recited in independent claim 13.' Examiner respectfully disagrees with Applicant.

16. In column 7, lines 52-60, Swoboda explicitly states that the two additional terminals nET1 and nET0 to the debug interface address the deficiency of 'IEEE standard does not support the parallel observation of internal chip activity or parallel stimulation of chip activity required for some test and emulation functionality'; therefore, these two terminals are used for testing and not during normal mode. See column 13, lines 10-54.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is

(703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00). I can be reached at a new number, (571) 272-3653, after October 15, 2004.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ROBERT BEAUSOLIEL
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